PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-236527

(43)Date of publication of application : 23.08.2002

(51)Int.Cl. G06F 1/26
G06F 1/24
G06F 15/177

(21)Application number : 2001-031698

(22)Date of filing : 08.02.2001

(71)Applicant : HITACHI LTD

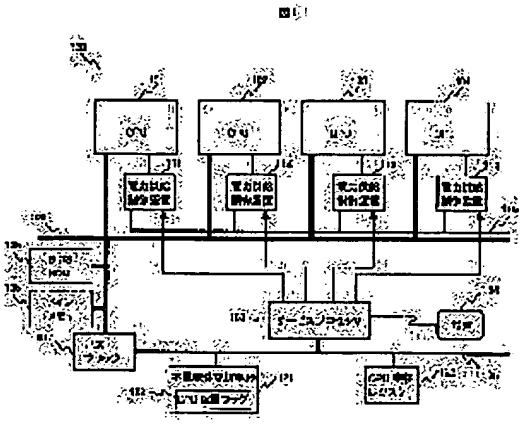
(72)Inventor : YAMAMOTO KOZO
OKAZAWA KOICHI

(54) MULTIPROCESSOR SYSTEM AND PROCESSOR CONTROL METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a multiprocessor system which can freely set whether some of mounted CPUs should be actuated.

SOLUTION: In a CPU operation flag 122 which is secured on a nonvolatile storage means 121, the constitution of processors to be operated is stored. A service processor 120 issues a power supply command to only the power supply controller of a processor to be operated among power supply controllers 111 to 114 for CPUs 101 to 104 according to the CPU operation flag 122 when an OS is started.



LEGAL STATUS

[Date of request for examination] 07.03.2005

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Two or more electric power supply control means which are the multiprocessor systems which have two or more processors, and control the electric power supply to said each processor, A setting means to set up the information about starting or a halt of each of said processor, A storage means to memorize the deactivation setting information about each processor set up by this setting means, The multiprocessor system characterized by providing the control means which takes out a command to said electric power supply control means based on this deactivation setting information, and controls the electric power supply of each of said processor in case said system is started.
[Claim 2] The multiprocessor system characterized by to provide a setting means to be the computer of the multiprocessor mold which has two or more processors, and to set up starting or a halt of each of said processor, a storage means memorize the deactivation setting information on said each processor set up by this setting means, and a means control reset for said every processor based on said deactivation setting information in case said system is started.
[Claim 3] It is the processor control approach which is the processor control approach which controls two or more processors, judges whether the user setting configuration about mounting of said processor is effective with reference to the mounting situation of two or more of said processors, and is characterized by memorizing this user setting configuration as a processor operation flag when this user setting configuration is effective as a result of this decision.
[Claim 4] the processor control approach according to claim 3 which reads said memorized processor operation flag, acquires the processor configuration which makes it work based on this result that carried out reading appearance, and is characterized by switching on and starting the power source of the this worked processor when starting said two or more processors.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the multiprocessor system which can choose CPU which actually starts in CPU mounted especially in the multiprocessor system which has two or more CPUs.
[0002]
[Description of the Prior Art] In recent years, the increment of the demand to the throughput of a computer is being enhanced, and adoption of the multiprocessor system which carries two or more CPUs is common as the technique of improvement in the speed of a computer in the server of which a high throughput is required by business youth called especially basic business and which is used. Moreover, when it stands on a position of a customer, since things can be carried out, a multiprocessor system has the merit for which a throughput is reinforced simply and which can use one computer over a long period of time by extending CPU, memory, and a hard disk, without a system buying, also when a customer's computer processing capacity increases. Generally such expandability is called scalability.
[0003] In a multiprocessor system, all CPUs carried are usually worked. The technique which controls the CPU configuration of a multiprocessor system is indicated by JP,8-221375,A. By this well-known example, by continuing inputting a reset signal to CPU which the failure generated, it considers as the condition of having separated the CPU concerned, only the processor which operates normally is chosen, and information processing system is rebooted. Moreover, by JP,11-202988,A, an operating system supervises the amount of use of each CPU, and the technique made to stop or suspend to CPU with few amounts of use is indicated. Thus, with the conventional technique about the CPU configuration control of a multiprocessor system, all CPUs carried work, and a system is started and degenerates CPU dynamically during system operation the time of a CPU failure, and for power saving. Generally in a multiprocessor system, the engine performance is determined by the number of CPU operation. For this reason, according to the Prior art, in order to change the processing engine performance as equipment of a multiprocessor system, the number of CPU mounting will be changed.
[0004]
[Problem(s) to be Solved by the Invention] In the above-mentioned multiprocessor system of the passage former, in order to offer the product which covers various throughputs and corresponds to a demand of a customer finely since it is the structure which works all CPUs mounted, a computer maker needs to prepare two or more models with which the numbers of CPU mounting differ also in the same model. For this reason, in a production process, it is necessary to form two or more production lines with the number of CPUs to carry, or to specify for a worker the number of CPUs carried by production instructions etc. with the same production line. Moreover, only a model number needs to perform device management in spite of the same device. Thus, offering various product lineup, in order to satisfy a customer's various needs by the Prior art will cause complication of a production process or device management.
[0005] Furthermore, CPU will be extended when the customer who already holds a multiprocessor

system reinforces the throughput of a system. Although goodness of scalability is made into the advantage of a multiprocessor system, it is not an easy activity to actually do the extension activity of CPU to a customer site. Considering the difficulty of CPU handling called increase of the number of pins accompanying reservation (it is hardly expectable that the computer private room is prepared in the server which is especially a business youth) of the work site in a customer site, complication of mounting in a case, and the own advanced features of CPU, it is technically difficult to do a CPU extension activity quickly. As a result, increase of the cost by a long duration halt of a customer job and long duration dispatch of a customer engineer will be caused.

[0006] This invention is made in view of the above-mentioned actual condition, CPU of a large number or the maximum number which can be mounted is mounted beforehand, and it aims at offering the multiprocessor system which can work only some CPUs in CPU mounted.

[0007]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, when this invention set up the information about starting or a halt of each processor, memorized the deactivation setting information about each set-up processor and started a system, in the multiprocessor system which has two or more processors, the configuration which controls the electric power supply of each processor based on said deactivation setting information was used for it. [0008]

[Embodiment of the Invention] Hereafter, the gestalt of the first operation in this invention is explained to a detail, referring to drawing 1 - drawing 5.

[0009] Drawing 1 shows the configuration of the multiprocessor system in the gestalt of the first operation. ROM in which, as for 101-104, CPU of this system was stored in, and, as for 105, the basic input/output system (BIOS) was stored, and 106 are bus bridges which connect the local bus 125 which main memory and 108 mention later with a system bus, and 107 mentions later with a system bus 108. Equipment for 111-114 to supply power to CPUs 101-104 and 115 are electric power supply lines. The service processor to which 120 performs the reset control and current supply control of CPU, and 121 are storage means of a non-volatile by which data are not eliminated at the time of a power source OFF, either. The nonvolatile memory and the hard disk drive unit which are called FLASH ROM can be considered. Moreover, the CPU operation flag 122 for recording the setting information on CPU that it is made to actually work in CPUs 101-104, in the non-volatile storage means 121 is stored. 123 is a register for extracting the CPU information actually carried in the multiprocessor system 100. 124 is the terminal connected with the service processor 120. 125 is a local bus which connects a service processor, and a shared memory and a CPU mounting register.

[0010] Drawing 2 shows the circuit about the CPU starting register 107 and the CPU mounting register 123 to a detail. The 1-bit information which CPU Slot 201-204 is insertion opening for carrying CPU to a multiprocessor system 100, and shows CPU mounting or un-mounting from Book Slot to the CPU mounting register 123 is transmitted. Drawing 3 is [an operation CPU configuration flag detail and drawing 5 of the setting processing flow of User Information and drawing 4] the starting processing flows of a system.

[0011] Although characterized by this invention starting a system with the CPU configuration according to a setup of a user in CPU mounted, the processing which registers first CPU which a user works is explained using the flow chart of drawing 3. A user chooses CPU which wants to work from CPU mounted through a terminal 124. It is confirmed whether a service processor 120 has the effective CPU configuration which extracted the CPU configuration mounted in the current multiprocessor system 100 from the CPU mounting register 123 (step 301), and the user chose (step 302). It is a step for checking whether this has chosen CPU in which the user is not mounted accidentally, or the configuration which does not have trouble in the electrical-characteristics top CPU operating has been chosen. And when a user sets up a normal configuration, a service processor 120 is stored in the CPU operation flag 122 which prepared the CPU operation configuration information specified by a user on the non-volatile storage means 121 (step 303), and the display which shows what a CPU operation setup of a user terminated normally is outputted to a terminal 124 (step 304). Here, the CPU operation flag 122 assigns operation of 1 bit, or the information that it does not work, for every CPU like a CPU mounting flag as it

is shown in drawing 4. "1" shows operation and "0" shows un-working. CPUs 101-103 are worked and a setup which presupposes un-working CPU104 is expressed with the example of drawing 4. Moreover, when a user chooses an unjust configuration, the display which shows that the demand of a user was not received the service processor 120 and it terminated abnormally is outputted to a terminal 124 (step 305). Setting up the CPU configuration worked to a multiprocessor system 100 by the above processing was completed. In addition, since the CPU operation flag 122 is stored on the non-volatile storage means 121, even if the power source of a multiprocessor system 100 is disconnected, the information on the CPU operation flag 122 is not eliminated. That is, if the CPU information worked once is set up at the time of installation, a user does not need to perform a setup, unless a CPU operation configuration is changed henceforth.

[0012] Next, the system startup processing which is based and performs a user setup is explained using the flow chart of drawing 5. A service processor 120 extracts the CPU operation flag 122 stored in the non-volatile storage means 121 (step 501), and publishes powering-on directions only to the power control of CPU worked in power control 111-114 according to it (step 502). For example, if based on drawing 4, a service processor 120 will publish powering-on directions to power control 111, 112, and 113. A power source is supplied only to CPU in which the user did an operation setup by this step. Next, a service processor 120 cancels a system reset (step 503), and CPU supplied in the power source starts it. According to this invention, only CPU which the user set up can be started above in CPU by which two or more loading is carried out.

[0013] Thereby, a computer maker can arrange various product lineup only by changing CPU which the model which mounted many CPUs beforehand is produced [CPU] and works it. Therefore, the difference in the number of CPU mounting at the time of production can be reduced, and a production stroke and device management can be simplified.

[0014] Next, the gestalt of the second operation in this invention is explained to a detail, referring to drawing 6 and drawing 7. Drawing 6 shows the gestalt of the second operation in this invention. In drawing 6, the same part as the gestalt of the first operation shown in drawing 1 attaches the same sign, and the explanation is omitted. As a new sign, 605 is equipment for supplying power to CPUs 101-104. Although power control exists in each CPU according to an individual in drawing 1, it controls by package with power control 605 at drawing 6. 631-634 are CPU reset control signal lines connected to the reset-signal input of CPUs 101-104. Drawing 7 is the starting processing flow of a multiprocessor system 600.

[0015] The processing which registers CPU which a user works is the same as that of drawing 3, and is omitted here. The system startup processing which is based and performs a user setup is explained using the flow chart of drawing 7. A service processor 120 extracts the CPU operation flag 122 stored in the non-volatile storage means 121 (step 701). Next, a service processor 120 publishes powering-on directions to power control 605 (step 702), and a power source is supplied to all CPUs carried. Next, according to a user setup of the CPU operation flag 122, only the CPU worked in CPUs 101-104 cancels CPU reset (step 703), and, as for a service processor 120, only CPU for a user setup starts it. Although energized with the gestalt of this operation also to CPU which does not work, there is no need of preparing power control for each CPU, and components mark can be lessened. By the way, although it continues inputting a CPU reset signal to CPU which does not work, the processing for ensuring a CPU halt may be added. For example, by having a disable signal input and inputting a disable signal to CPU which does not work, CPU becomes invalid and CPU can ensure a halt in part.

[0016]

[Effect of the Invention] In the multiprocessor system of this invention, CPU started in CPU mounted can be freely set up as explained above.

[0017] Moreover, in the multiprocessor system of this invention, in a CPU extension activity, since a CPU extension activity can be ended only by changing the number of operation CPUs into a system, without doing an actual CPU loading activity, a customer can avoid a prolonged job halt and special customer engineer dispatch, and can reduce cost.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the gestalt of operation of the first of this invention.
[Drawing 2] The block diagram of the CPU mounting register 123.
[Drawing 3] The flow chart which shows the procedure of setting a CPU operation configuration as a multiprocessor system 100.
[Drawing 4] The mimetic diagram showing the detail of the CPU operation flag 122.
[Drawing 5] The flow chart which shows the procedure with which the service processor 120 in the gestalt of the first operation starts CPU.
[Drawing 6] The block diagram showing the configuration of the second of the gestalt of operation of this invention.
[Drawing 7] The flow chart which shows the procedure with which the service processor 120 in the gestalt of the second operation starts CPU.
[Description of Notations]
100: A multiprocessor system, 101-104:CPU, 105:BIOS ROM, 106:main memory, a 107:bus bridge, a 108:system bus, a 111 - 114:current supply control device, a 115:electric power supply line, a 120:service processor, a 121:non-volatile storage means, a 122:CPU operation flag, a 124:CPU mounting register, a 125:local bus, 201 - 204:CPU Slot, a 400:CPU operation flag, a 600:multiprocessor system, 605 : an electric power supply control device, a 631 - 634:CPU reset control signal line

---

[Translation done.]

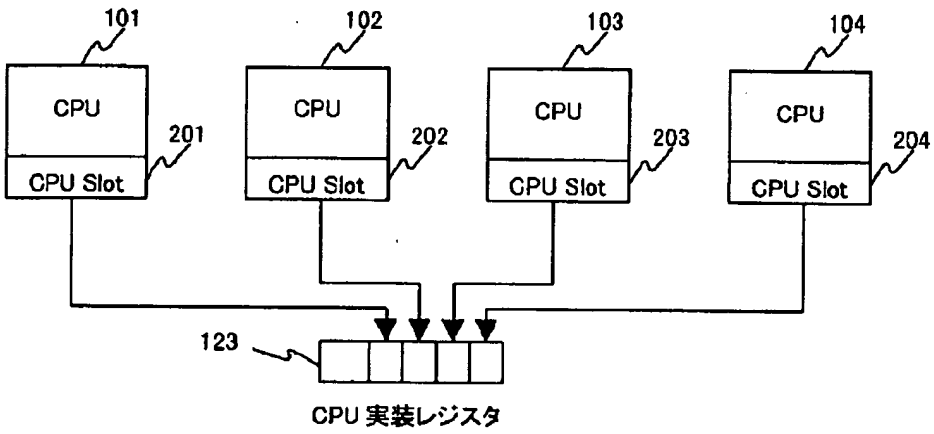
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

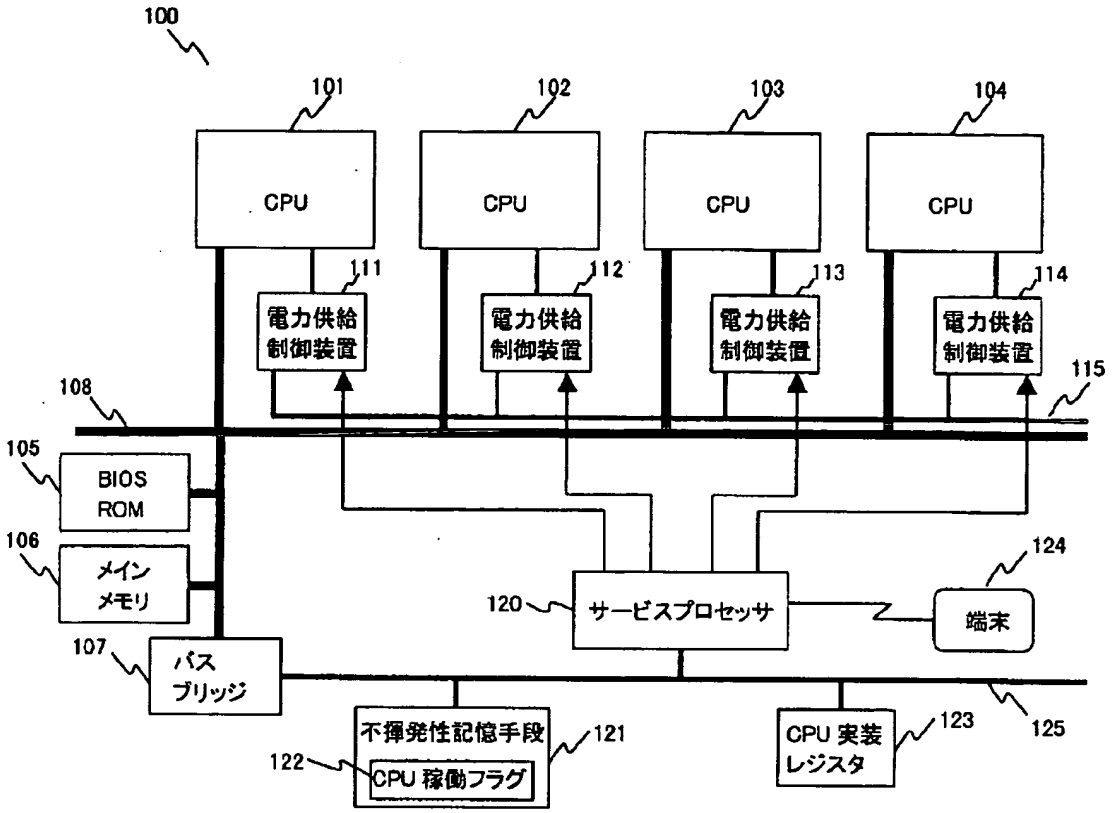
[Drawing 2]

図 2



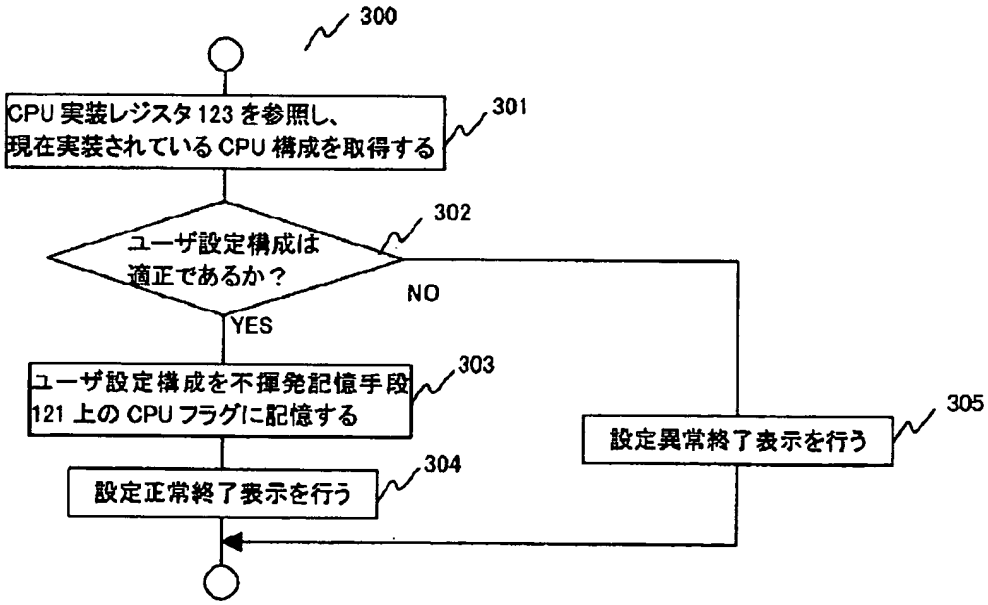
[Drawing 1]

図 1



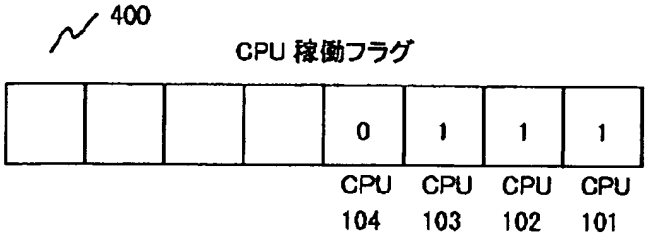
[Drawing 3]

図 3



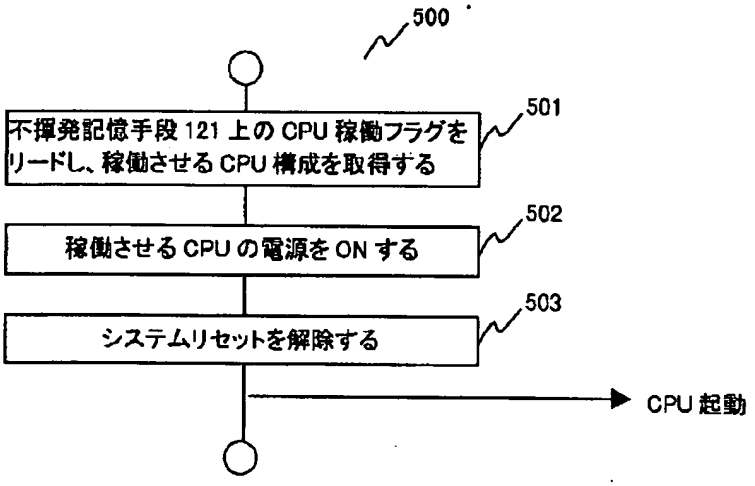
[Drawing 4]

図 4



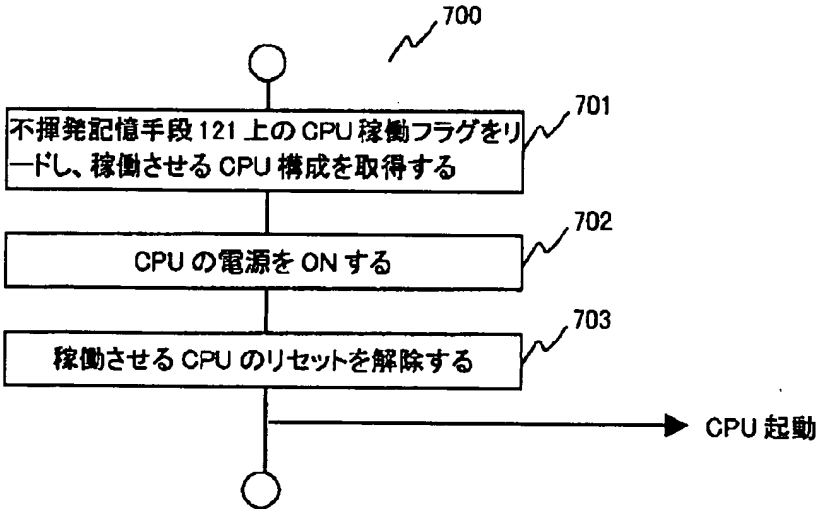
[Drawing 5]

図 5



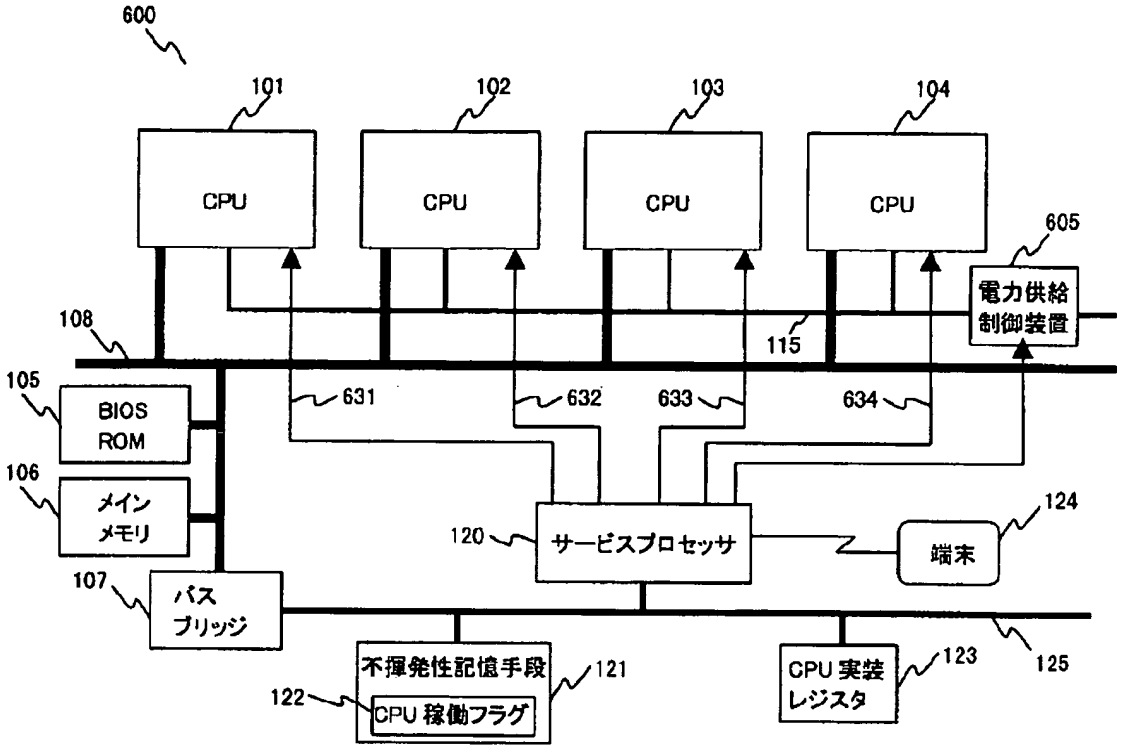
[Drawing 7]

図 7



[Drawing 6]

図6



[Translation done.]